# Data Sheet

<table>
<thead>
<tr>
<th>Module Type</th>
<th>DDR4 4GB/8GB/16GB ECC UDIMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module speed</td>
<td>PC4-17000</td>
</tr>
<tr>
<td>Pin</td>
<td>288 pin</td>
</tr>
<tr>
<td>Cl-tRCD-tRP</td>
<td>15-15-15</td>
</tr>
<tr>
<td>SDRAM Operating Temp</td>
<td>0℃~85℃</td>
</tr>
</tbody>
</table>
1. **Features**

<table>
<thead>
<tr>
<th>Industry Nomenclature</th>
<th>Speed Grade</th>
<th>Data Rate MT/s</th>
<th>tRCD (ns)</th>
<th>tRP (ns)</th>
<th>tRC (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC4-17000 R</td>
<td>CL=11</td>
<td>1600</td>
<td>14.06</td>
<td>14.06</td>
<td>47.06</td>
</tr>
<tr>
<td></td>
<td>CL=13</td>
<td>1866</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CL=15</td>
<td>2133</td>
<td></td>
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</tbody>
</table>

- JEDEC Standard 288-pin Dual In-Line Memory Module
- Intend for PC4-17000 applications
- Inputs and Outputs are SSTL-12 compatible
- \( V_{DD} = V_{DDQ} = 1.2 \) Volt (TYP)
- \( V_{PP} = 2.5 \) Volt (TYP)
- \( V_{DDSPD} = 2.2-3.6V \)
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector
- Fly-By topology
- Golden Connector
- Terminated control, command and address bus
- Programmable /CAS Latency: 11, 13, 15
- Operation temperature – \((0^\circ C - 85^\circ C)\)
- On-die VREFDQ generation and Calibration
- On-Board EEPROM
- ECC Function
- RoHs and Halogen free (*Section 13*)
2. PACKAGE DIMENSION

Note:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.